CLAIM LISTING

1. (Previously Presented) A video decoder for decoding macroblocks, said video decoder comprising:

a processor for decoding a set of parameters, said set of parameters comprising motion vectors indicating reference pixels associated with the macroblock;

a frame buffer for storing past and future reference pictures;

a motion vector address computer for calculating addresses associated with motion vectors;

a video request manager for fetching a block of reference pixels at the addresses from the frame buffer that were calculated by the motion vector address computer; and

a pixel reconstructor for reconstructing pixels from the macroblocks, the pixel reconstructor operable to reconstruct pixels from macroblocks encoded in accordance with a plurality of standards, said pixel reconstructor further comprising:

a macroblock input buffer for storing the reference pixels that are fetched from the frame buffer by the video request manager at the addresses calculated by the motion vector address computer; and

a register for storing a portion of the reference pixels that are fetched from the frame buffer by

the video request manager at the addresses calculated by the motion vector address computer; and

wherein the register, macroblock input buffer, and frame buffers are separate.

2. (Original) The video decoder of claim 1, wherein the plurality of standards comprises MPEG-2 and AVC.

3. (Cancelled).

4. (Previously Presented) The video decoder of claim 1, wherein the pixel reconstructor comprises:

a data path for outputting another portion of the reference pixels.

5. (Previously Presented) A pixel reconstructor for decoding macroblocks, said pixel reconstructor comprising:

a macroblock input buffer for storing reference pixels that are referenced by at least one motion vector;

a multiplexer connected to the macroblock input buffer;

a register connected to the multiplexer for storing a portion of the reference pixels that are referenced by the at least one motion vector; and

a data path connected in parallel to the register.

6. (Original) A pixel reconstructor of claim 5, further comprising:

a macroblock input buffer register connected to the multiplexer.

7. (Previously Presented) A pixel reconstructor of claim 6, further comprising:

another multiplexer connected to the register.

8. (Original) The pixel reconstructor of claim 7, further comprising:

a bypass path connected to the macroblock input buffer and the another multiplexer, said bypass path bypassing the multiplexer and the multiplexer input buffer register.

9. (Original) The pixel reconstructor of claim 8 to reconstruct pixels from macroblocks encoded in accordance with a plurality of standards.

10. (Original) The pixel reconstructor of claim 9, wherein the plurality of standards comprises MPEG-2 and AVC.

11. (New) The video decoder of claim 1, wherein:

during a first cycle:

the register stores reference pixels for a first half of a row of a luma portion of a macroblock;

the pixel reconstructor applies offsets to said reference pixels for the first half of the row of the luma portion of the macroblock, thereby resulting in the first half of the row of the luma portion of the macroblock.

12. (New) The video decoder of claim 11, wherein:

during a second cycle:

the register outputs the first half of the row of the luma portion of the macroblock and receives reference pixels for the second half of a row of luma portion of a macroblock; and

the pixel reconstructor applies offsets to said reference pixels for the second half of the row of the luma portion of the macroblock, thereby resulting in the second half of the row of the luma portion of the macroblock.